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10/560,408	12/12/2005	Kauko O. Laakkonen	915-001.074	5474

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EXAMINER	
CRAWFORD, JACINTA M	
ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/560,408	LAAKKONEN, KAUKO O.	
	Examiner	Art Unit	
	JACINTA CRAWFORD	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9 and 11-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9 and 11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 3, 4, 6-9, 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Valentaten et al. in view of Niimura et al.

With respect to claim 1, Valentaten et al. teach the claimed intelligent display device connection interface integrated in the display device, at figure 2 the video circuit 16; a memory bus connected to the processor in order to realize signaling between the processor and the display device connection interface, at figure 2, the bus between the processor 14 and the RAM arbiter 18; and an adapter circuit, the RAM arbiter 18 in figure 2, in order to match signals between the memory bus and the display device connection interface, with the arbiter controlling the access to the memory bus, thereby matching the timing of the signals.

Valentaten et al. teaches at column 4 lines 30-35 the adapter circuit to include means for synchronizing the signals of the memory bus in an order required by the display device.

While Valentaten et al. teaches most features claimed, it is noted that figure 2 does not explicitly show a display device. However, Niimura et al. teaches a similar arrangement and shows the display at figure 5 item 9. It would have been obvious to one of ordinary skill in the art to determine the presence of a display because Valentaten et al. shows connections to the video circuit 16 and also discusses this at column 4 lines 5-7.

Claim 8 is similar to claim 1 but is drafted in method form. Claim 8 is rejected based on the rationale presented for the rejection of claim 1 for similar respective features.

Claim 12 is similar to claim 1 but is broader in scope, and is rejected under similar rationale presented for the rejection of claim 1

Claim 3 further requires the memory bus connected to the processor to be a non- synchronized memory bus. Niimura et al. teach this at the abstract.

Claim 4 further requires the memory bus to before realizing signaling between the processor and a memory unit, as well as between the processor and the display device connection interface. Niimura et al. teach this at figure 5.

Claim 6 further requires the adapter circuit to be provided with gates in order to match the signals between the memory bus and the connection interface. This would have been obvious to

one of ordinary skill 'in the art because logic gates are an integral part of digital circuitry.

Claim 7 further requires the arrangement to also include an interference protection segment in order to prevent electric interference. The instant specification describes this as known.

Claim 9 further requires the memory bus connected to the processor to be arranged to function both as a bus between the processor and a memory unit, and a bus between the processor and the display device. Niimura et al. shows this at figure 5.

Claim 11 further requires the memory bus and the display device connection interface to be connected by glue logics together in order to achieve communication there between. This is directly apparent at Valentaten et al. at figure 2.

Claim 13 further requires the adapter circuit to be provided with gates for synchronizing the timing of the signals between the display device connection interface and the memory bus, and for combining the connection interface and the memory bus as a physical, uniform bus. This is similar to claim 6 and is rejected under similar rationale, also taking into account figure 5 of Niimura et al.

Claim 14 is similar to claim 6 and is rejected under similar rationale.

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Valentaten et al. in view of Niimura et al. as applied to claim 1 above, and further in view of Leung.

Claim 2 requires the display device connection interface to be a medium speed screen interface. While Valentaten et al. is used to a display device connection, it is noted that Valentaten does not express a medium speed screen interface. However, Leung teaches the use of low medium and high speed interfaces at column 9, lines 36-39, 56-67 and column 10, lines 8-10. It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the system to have a medium speed screen interface to facilitate proper establish communication among the devices.

Response to Arguments

4. Applicant's arguments filed August 15, 2008 have been fully considered but they are not persuasive. Applicant amends independent claims 1, 8, and 12 to recite similar limitations as cancelled claim 5. Applicant argues on pages 6 and 7 of the amendment filed that the adapter circuit recited in independent claims 1, 8, and 12 is different from the RAM arbiter disclosed by Valentaten et al. where the RAM arbiter does not disclose signals are synchronized by the RAM arbiter in an order required by the video display. However, Valentaten et al. disclose the RAM arbiter to resolve contention for the memory by controlling and prioritize accesses to the memory. The video circuit 16 which is considered the "display device connection interface" is used to generate signals and different monitor screen types for the monitor. The embedded

processor 14 which is considered "processor" controls the video circuit 16 and performs various function and operations such as generating data to for video circuit 16 for the display monitor. RAM is a shared memory which is accessed by both video circuit and processor. However, the RAM arbiter can identify the appropriate RAM bus cycles within which to execute video function accesses to RAM where the video circuit is able to continuously update the monitor by accessing data via the RAM arbiter without conflicting with the processor. Therefore, the system meets the desired balance needed between screen rate and RAM bus utilization (see, column 3, lines 31 thru column 4, lines 65).

Applicant argues on page 8 with respect to claim 2 regarding the trademark "Nokia Oyj". The 35 USC 112, 2nd paragraph of claim 2 has been withdrawn due to *current* amendment and is now rejected in view of Leung.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JACINTA CRAWFORD whose telephone number is (571)270-1539. The examiner can normally be reached on M-F 8:00a.m. - 5:00p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jacinta Crawford/
Examiner, Art Unit 2628

/Kee M Tung/
Supervisory Patent Examiner, Art Unit 2628